VTM706P/R/S/T/J, VTM708R/S/T/J

3/3.3/4.0V µP Supervisor Circuits

- **Low supply current**
- **Watchdog timer**
- **Brownout detection**

The VTM706P/R/S/T/J and VTM708R/S/T/J CMOS supervisor circuits monitor power-supply and battery voltage level, and µP/µC operation.A reset is generated when the supply drops below 2.63V (VTM706P/R,VTM708R), 2.93V (VTM706S, VTM708S), 3.08V (VTM706T, VTM708T) or 4.00 (VTM706J, VTM708J).

The family offers several functional options. Each device generates a reset signal during power-up, power-down and during brownout conditions.

In addition, the VTM706P/R/S/T/Jfeature a 1.6 second watchdog timer .The watchdog timer output will trigger a reset if connected to MR Unlike competitive devices, floating the WDI input pin disables the watchdog timer.

The VTM708R/S/T/J have both active-HIGH and active-LOW reset outputs but no watchdog function. The VTM706P has the same pin-out and functions as the VTM706R but has an active-HIGH reset output.

A versatile power-fail circuit, useful in checking battery levels and non-5V supplies, has a 1.25V threshold. All devices have a manual reset input.

All devices are available in 8-pin DIP, SO and the compact MicroSO packages. The MicroSO package requires 50% less PC board area than the conventional SO package.

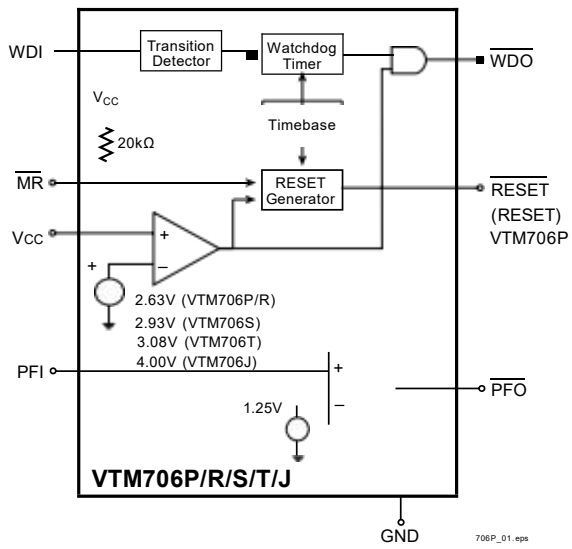
Key Features

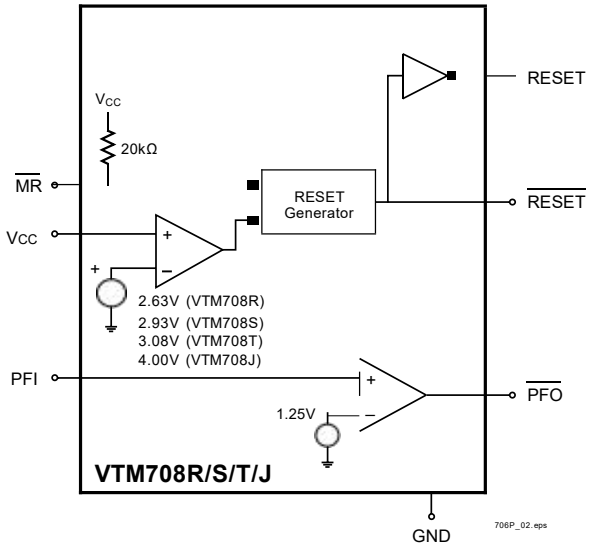
- Lower power, pincompatible replacements for Maxim MAX706P/R/S/T, MAX708R/S/T
  - 30% lower supply current:140µA vs. 200µA
- Precision power supply monitor
  - 2.63V threshold (VTM706P/R, VTM708R)
  - 2.93V threshold (VTM706S, VTM708S)
  - 3.08V threshold (VTM706T, VTM708T)
  - New 4.00V threshold (VTM706J,VTM708J)
- Debounced manual reset input
- Auxiliary voltage monitor comparator
  - 1.25V threshold
  - Battery monitor/auxiliary supply monitor
- Watchdog timer (VTM706P/R/S/T/J)
  - Watchdog can be disabled by floating WDI
- 200ms reset time delay
- Three reset signal options
  - Active HIGH: VTM706P
  - Active LOW: VTM706R/S/T/J
  - Active HIGH & LOW outputs: VTM708R/S/T/J
- DIP, SO and MicroSO packages
- Guaranteed RESET assertion to V_{CC} = 1.1V

Applications

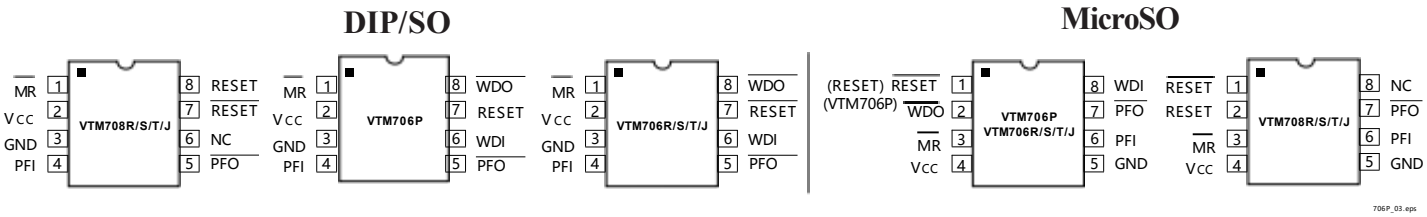
- Computers and controllers
- CTI applications
- Embedded controllers
- Battery operated systems
- Intelligent instruments
- Wireless communication systems
- PDAs and handheld equipment

Block Diagrams





Pin Configuration



Ordering Information

Part Number	Package	Operating Temperature Range	Reset Threshold	Reset Polarity	Watchdog Timer
VTM706PCPA	8-Plastic DIP	0。C to +70。C	2.63	HIGH	YES
VTM706PCSA	8-SO	0。C to +70。C	2.63	HIGH	YES
VTM706PCUA	8-MicroSO	0。C to +70。C	2.63	HIGH	YES
VTM706PEPA	8-Plastic DIP	–40。C to +85。C	2.63	HIGH	YES
VTM706PESA	8-SO	–40。C to +85。C	2.63	HIGH	YES
VTM706RCPA	8-Plastic DIP	0。C to +70。C	2.63	LOW	YES
VTM706RCSA	8-SO	0。C to +70。C	2.63	LOW	YES
VTM706RCUA	8-MicroSO	0。C to +70。C	2.63	LOW	YES
VTM706REPA	8-Plastic DIP	–40。C to +85。C	2.63	LOW	YES
VTM706RESA	8-SO	–40。C to +85。C	2.63	LOW	YES
VTM706SCPA	8-Plastic DIP	0。C to +70。C	2.93	LOW	YES
VTM706SCSA	8-SO	0。C to +70。C	2.93	LOW	YES
VTM706SCUA	8-MicroSO	0。C to +70。C	2.93	LOW	YES
VTM706SEPA	8-Plastic DIP	–40。C to +85。C	2.93	LOW	YES
VTM706SESA	8-SO	–40。C to +85。C	2.93	LOW	YES
VTM706TCPA	8-Plastic DIP	0。C to +70。C	3.08	LOW	YES
VTM706TCSA	8-SO	0。C to +70。C	3.08	LOW	YES
VTM706TCUA	8-MicroSO	0。C to +70。C	3.08	LOW	YES
VTM706TEPA	8-Plastic DIP	–40。C to +85。C	3.08	LOW	YES
VTM706TESA	8-SO	–40。C to +85。C	3.08	LOW	YES
VTM706JCPA	8-Plastic DIP	0。C to +70。C	4.00	LOW	YES
VTM706JCSA	8-SO	0。C to +70。C	4.00	LOW	YES
VTM706JCUA	8-MicroSO	0。C to +70。C	4.00	LOW	YES
VTM706JEPA	8-Plastic DIP	–40。C to +85。C	4.00	LOW	YES
VTM706JESA	8-SO	–40。C to +85。C	4.00	LOW	YES
VTM708RCPA	8-Plastic DIP	0。C to +70。C	2.63	Dual: HIGH & LOW	NO
VTM708RCSA	8-SO	0。C to +70。C	2.63	Dual: HIGH & LOW	NO
VTM708RCUA	8-MicroSO	0。C to +70。C	2.63	Dual: HIGH & LOW	NO
VTM708REPA	8-Plastic DIP	–40。C to +85。C	2.63	Dual: HIGH & LOW	NO
VTM708RESA	8-SO	–40。C to +85。C	2.63	Dual: HIGH & LOW	NO
VTM708SCPA	8-Plastic DIP	0。C to +70。C	2.93	Dual: HIGH & LOW	NO
VTM708SCSA	8-SO	0。C to +70。C	2.93	Dual: HIGH & LOW	NO
VTM708SCUA	8-MicroSO	0。C to +70。C	2.93	Dual: HIGH & LOW	NO
VTM708SEPA	8-Plastic DIP	–40。C to +85。C	2.93	Dual: HIGH & LOW	NO
VTM708SESA	8-SO	–40。C to +85。C	2.93	Dual: HIGH & LOW	NO
VTM708TCPA	8-Plastic DIP	0。C to +70。C	3.08	Dual: HIGH & LOW	NO
VTM708TCSA	8-SO	0。C to +70。C	3.08	Dual: HIGH & LOW	NO
VTM708TCUA	8-MicroSO	0。C to +70。C	3.08	Dual: HIGH & LOW	NO
VTM708TEPA	8-Plastic DIP	–40。C to +85。C	3.08	Dual: HIGH & LOW	NO
VTM708TESA	8-SO	–40。C to +85。C	3.08	Dual: HIGH & LOW	NO
VTM708JCPA	8-Plastic DIP	0。C to +70。C	4.00	Dual: HIGH & LOW	NO
VTM708JCSA	8-SO	0。C to +70。C	4.00	Dual: HIGH & LOW	NO
VTM708JCUA	8-MicroSO	0。C to +70。C	4.00	Dual: HIGH & LOW	NO
VTM708JEPA	8-Plastic DIP	–40。C to +85。C	4.00	Dual: HIGH & LOW	NO
VTM708JESA	8-SO	–40。C to +85。C	4.00	Dual: HIGH & LOW	NO

Absolute Maximum Ratings

Pin Terminal Voltage with Respect to Ground
V_{CC} . . . . . –0.3V to 6.0V

All other inputs . . . . . –0.3V to (V_{CC}+0.3V) °C
Input Current at V_{CC} and GND 20mA
Output Current: All outputs 20mA
Rate of Rise at V_{CC} 100V/µs
Plastic DIP Power Dissipation 700mW
(Derate 9mW/°C above 70°C)
SO Power Dissipation 470mW
(Derate 5.9mW/°C above 70°C)
MicroSO Power Dissipation 330mW
(Derate 4.1mW/°C above 70°C)

Operating Temperature Range
VTM706xE, VTM708xE . . . . . –40°C to +85

VTM706xC, VTM708xC . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +160°C
Lead Temperature Soldering (10 sec) . . . . . 300°C

These are stress ratings only and functional operation is not VTMlied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.

Electrical Characteristics

Typical values at Ta=25 °C,V_{CC} supply voltages are 3.0V to 5.5V (VTM706P, VTM708R), 3.3V to 5.5V (VTM706/8S), 3.5V to 5.5V (VTM706/8T) and 5.0V to 5.5V (VTM706/8J).

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Voltage Range	V_{CC}	VTM706xC, VTM708xC VTM706xE, VTM708xE	1.1 1.2		5.5 5.5	V
Supply Current V_{CC} < 3.6V	I_{CC}	VTM706xC, VTM706xE, $\overline{MR}$ = V_{CC},WDI Floating		75	140	µA
		VTM708xC, VTM708xE, $\overline{MR}$ =V_{CC}, WDI Floating		50	140	
Supply Current V_{CC} < 5.5V	I_{CC}	VTM706xC, VTM706xE,$\overline{MR}$ = V_{CC}, WDI Floating		75	140	µA
		VTM708xC, VTM708xE, $\overline{MR}$ = V_{CC}, WDI Floating		50	140	
RESET Threshold	V_{RT}	P and R devices S devices T devices J devices	2.55 2.85 3.00 3.89	2.63 2.93 3.08 4.00	2.70 3.00 3.15 4.10	V
RESET Threshold Hysteresis				40		mV
RESET Pulse Width	t_{RS}	V_{CC} = 3V (VTM706/8, P/R devices), V_{CC} = 3.3V (VTM706/8, S/T devices) V_{CC} = 4.4V (VTM706/8,J devices)	140	200	280	ms
		V_{CC} = 5V		200		
$\overline{MR}$ Pulse Width	t_{MR}	4.5V < V_{CC} < 5.5V	150			ns
		3.6V < V_{CC} < 4.5V (VTM706/8J devices) $V_{RST\ (MAX)}$ < V_{CC} < 3.6V (VTM706/8P/R/S/T devices)	500			
$\overline{MR}$ to RESET Out Delay	t_{MD}	3.6V < V_{CC} < 4.5V (VTM706/8J devices) $V_{RST(MAX)}$ < V_{CC} < 3.6V (VTM706/8P/R/S/T devices)			750	ns
		4.5V < V_{CC} < 5.5V			250	
$\overline{MR}$ Input Threshold	V_{IH}	$V_{RST\ (MAX)}$ < V_{CC} < 4.5V	0.7V_{CC}			V
	V_{IL}	$V_{RST\ (MAX)}$ < V_{CC} < 4.5V			0.6	
	V_{IH}	4.5V < V_{CC} < 5.5V	2.0			
	V_{IL}	4.5V < V_{CC} < 5.5V			0.8	
$\overline{MR}$ Pull-up Resistor	R_P		10	20	40	kΩ
$\overline{RESET}$ Output Voltage (All R/S/T/J devices)	V_{OH}	I_{SOURCE}= 800µA, 4.5V < V_{CC} < 5.5V	V_{CC}–1.5V			V
	V_{OL}	I_{SINK} = 3.2mA, 4.5V < V_{CC} < 5.5V			0.4	
	V_{OH}	I_{SOURCE}= 500µA, $V_{RST\ (MAX)}$ < V_{CC} < 4.5V	0.8 V_{CC}			
	V_{OL}	I_{SINK} = 1.2mA, $V_{RST\ (MAX)}$ < V_{CC} < 4.5V			0.3	
	V_{OL}	I_{SINK}= 50µA, V_{CC} = 1.1(VTM706xC,VTM708xC devices)			0.3	
		I_{SINK}= 100µA, V_{CC} = 1.2V (VTM706xE, VTM708xE devices)			0.3	

Electrical Characteristics (cont.)

Unless otherwise noted, specifications are over the operating temperature range and V_{CC} supply voltages are 2.7V to 5.5V (VTM706P ,VTM708R), 3.0V to 5.5V (VTM706/8S), 3.15V to 5.5V (VTM706/8T) and 4.1V to 5.5V (VTM706/8J).

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESET Output Voltage VTM706P	V_{OH}	I_{SOURCE} = 800µA, 4.5V < V_{CC}< 5.5V	V_{CC}–1.5V			V
	V_{OL}	I_{SINK} = 3.2mA, 4.5V < V_{CC}< 5.5V			0.4	
	V_{OH}	I_{SOURCE} = 500µA, $V_{RST\ (MAX)}$ < V_{CC}< 3.6V	0.8V_{CC}			
	V_{OL}	I_{SINK} = 1.2mA, $V_{RST\ (MAX)}$ < V_{CC}< 3.6V			0.3	
RESET Output Voltage, VTM708R/S/T/J	V_{OH}	I_{SOURCE} = 800µA, 4.5V < V_{CC}< 5.5V	V_{CC}–1.5V			V
	V_{OL}	I_{SINK} = 3.2mA, 4.5V < V_{CC}< 5.5V			0.4	
	V_{OH}	I_{SOURCE} = 500µA, $V_{RST\ (MAX)}$ < V_{CC}< 4.5V	0.8V_{CC}			
	V_{OL}	I_{SINK} = 1.2mA, $V_{RST\ (MAX)}$ < V_{CC}< 4.5V			0.3	
Watchdog Timeout Period	t_{WD}	V_{CC}= 3V (VTM706, P/R devices) V_{CC} = 3.3V (VTM706, S/T devices) V_{CC} = 4.4V (VTM706, J devices)	1.0	1.6	2.25	s
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}, $V_{RST\ (MAX)}$ < V_{CC}< 4.5V	100			ns
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}, 4.5V < V_{CC}< 5.5V	50			ns
WDI Input Threshold	V_{IH}	V_{CC} = 5V	3.5			V
	V_{IL}				0.8	
	V_{IH}	$V_{RST\ (MAX)}$ < V_{CC}< 4.5V	0.7V_{CC}			
	V_{IL}				0.6	
WDI Input Current		WDI = V_{CC}, VTM706 Only		50	150	µA
WDI Input Current		WDI = 0V, VTM706 Only	–150	–50		µA
$\overline{WDO}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA, 4.5V < V_{CC}< 5.5V	V_{CC}–1.5V			V
	V_{OL}	I_{SINK} = 1.2mA, 4.5V < V_{CC}< 5.5V			0.4	
	V_{OH}	I_{SOURCE} = 500µA, $V_{RST\ (MAX)}$ < V_{CC}< 4.5V	0.8V_{CC}			
	V_{OL}	I_{SINK} = 500µA, $V_{RST\ (MAX)}$ < V_{CC}< 4.5V			0.3	
PFI Input Threshold		PFI falling. For P/R devices Vcc = 3V. For S/T devices Vcc = 3.3V. For J devices V_{CC} = 4.4V.	1.2	1.25	1.3	V
PFI Input Current			–25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA, 4.5V < V_{CC}< 5.5V	V_{CC}–1.5V			V
	V_{OL}	I_{SINK} = 3.2mA, 4.5V < V_{CC}< 5.5V			0.4	
	V_{OH}	I_{SOURCE} = 500µA, $V_{RS\ (MAX)}$ < V_{CC}< 4.5V	0.8V_{CC}			
	V_{OL}	I_{SINK} = 1.2mA, $V_{RS\ (MAX)}$ < V_{CC}< 4.5V			0.3	

Pin Descriptions

Pin Number						Name	Function
VTM706P		VTM706R/S/T/J		VTM708R/S/T/J			
DIP/SO	MicroSO	DIP/SO	MicroSO	DIP/SO	MicroSO		
1	3	1	3	1	3	$\overline{MR}$	Manual reset input. The active LOW input triggers a reset pulse. It is pulled HIGH by a 20kΩ pull-up resistor. It is compatible with TTL/CMOS signals when V_{CC} = 5V. It can be shorted to ground through a mechanical switch. Leave floating or connect to V_{CC} if the function is not used.
2	4	2	4	2	4	V_{CC}	Monitored power supply input.
3	5	3	5	3	5	GND	Ground
4	6	4	6	4	6	PFI	Power-fail input voltage monitor. With PFI less than 1.25V, PFO goes LOW. Connect PFI to ground when not used.
5	7	5	7	5	7	$\overline{PFO}$	Power-fail output. The output is active LOW and sinks current when PFI is less than 1.25V. If not used, leave the pin unconnected.
6	8	6	8	—	—	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6 sec at WDI allows the internal timer to run-out, setting WDO low. A rising or falling edge must occur at WDI within 1.6 seconds or WDO goes LOW. The watchdog function is disabled by floating WDI. The internal watchdog timer clears when: RESET is asserted; WDI is three-stated; or WDI sees a rising or falling edge.
—	—	—	—	6	8	NC	Not connected.
—	—	7	1	7	1	$\overline{RESET}$	Active-LOW reset output. Pulses LOW for 200ms when triggered, and stays LOW whenever V_{CC} is below the reset threshold. RESET remains LOW for 200ms after V_{CC} rises above the RESET threshold or MR goes from HIGH to LOW. A watchdog timeout will not trigger RESET unless WDO is connected to MR.
8	2	8	2	—	—	$\overline{WDO}$	Watchdog output. $\overline{WDO}$ goes LOW when the 1.6 second internal watchdog timer times-out and does not go HIGH until a transition occurs at WDI. In addition,when V_{CC} falls below thereset threshold, WDO goes LOW. Unlike RESET, WDO does not have a minimum pulse width and as soon as V_{CC} exceeds thereset threshold,WDO becomes HIGH with no delay.
7	1	—	—	8	2	RESET	Active-HIGH reset output. RESET is the inverse of $\overline{RESET}$.

Feature Summary

	VTM706P	VTM706R	VTM706S	VTM706T	VTM706J	VTM708R	VTM708S	VTM708T	VTM708J
Power-fail detector	■	■	■	■	■	■	■	■	■
Brownout detection	■	■	■	■	■	■	■	■	■
Debounced manual RESET input	■	■	■	■	■	■	■	■	■
Power-up/down RESET	■	■	■	■	■	■	■	■	■
Watchdog timer	■	■	■	■	■				
Active-HIGH RESET	■								
Active-LOW RESET		■	■	■	■				
Active-LOW and HIGH RESETs						■	■	■	■
RESET threshold	2.63V	2.63V	2.93V	3.08V	4.00V	2.63V	2.93V	3.08V	4.00V

Detail Descriptions

RESET/RESET Operation

The RESET/$\overline{\text{RESET}}$ signals are designed to start or return a μP/μC to a known state.

With V_{CC} above 1.2V, RESET and $\overline{\text{RESET}}$ are guaranteed to be asserted. During a power-up sequence, the reset outputs remain asserted until the supply rises above the threshold level. The resets are deasserted approximately 200ms after crossing the threshold.

In a brownout situation where V_{CC} falls below the threshold level, the reset outputs are asserted. If a brownout occurs during an already initiated reset period, the reset period will extend for an additional reset period of 200ms.

The VTM708 devices have dual reset outputs, one active LOW and one active HIGH. The VTM706P has a single active HIGH reset and the VTM706/R/S/T/J devices have an active LOW reset output.

VTM Part	RESET Polarity	Threshold	Watchdog Timer
VTM706P	HIGH	2.63V	Yes
VTM706R	LOW	2.63V	Yes
VTM706S	LOW	2.93V	Yes
VTM706T	LOW	3.08V	Yes
VTM706J	LOW	4.00V	Yes
VTM708R	Both: HIGH & LOW	2.63V	No
VTM708S	Both: HIGH & LOW	2.93V	No
VTM708T	Both: HIGH & LOW	3.08V	No
VTM708J	Both: HIGH & LOW	4.00V	No

Manual Reset ($\overline{\text{MR}}$)

The active-LOW manual reset input is pulled high by an internal 20kΩ pull-up resistor and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140ms minimum reset time will debounce mechanical pushbuttonswitches. The minimum MR input pulse width is 0.5μs with a 3V V_{CC} input and 0.15μs with a 5V V_{CC} input. If not used, tie MR to V_{CC} or leave floating.

By connecting the watchdog output ($\overline{\text{WDO}}$) and $\overline{\text{MR}}$, a watchdog timeout forces a RESET to be generated.

Watchdog Timer

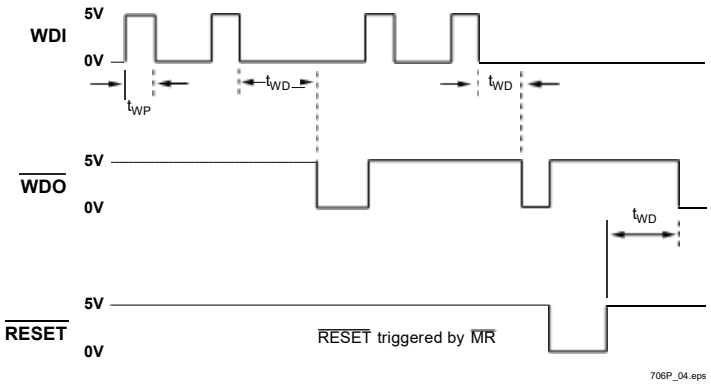
A watchdog timer available on the VTM706P/R/S/T/J monitors μP/μC activity. If activity is not detected within 1.6 seconds on the Watchdog Input (WDI), the internal timer puts the Watchdog Output (WDO) into a LOW state. WDO will remain LOW until activity is detected at WDI.

The watchdog function is disabled, meaning it is cleared and not counting, if WDI is floated or connected to a three-stated circuit. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 100ns (V_{CC} = 2.7V)/50ns (V_{CC} = 4.5V), the watchdog timer will begin a 1.6 second countdown. Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

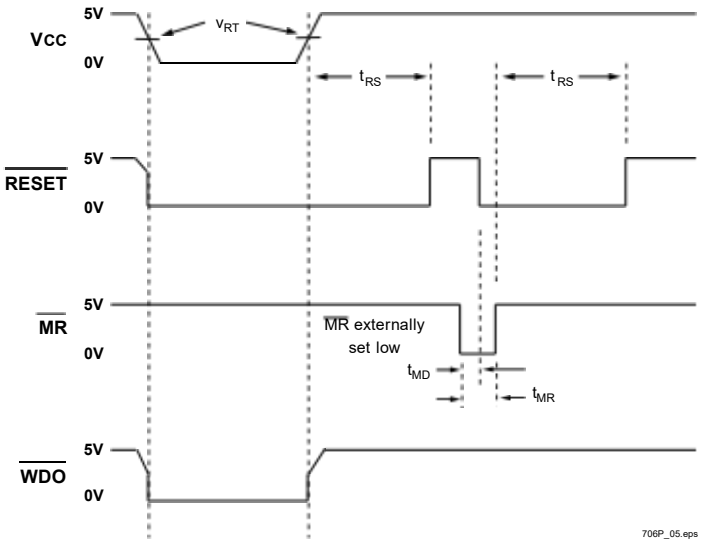
$\overline{\text{WDO}}$ will also become LOW and remain so, whenever the supply voltage,V_{CC}, falls below the device threshold level. WDO goes HIGH as soon as V_{CC} transitions above the threshold. There is no minimum pulse width for WDO as there is for theRESET outputs. If WDI is floated,WDO essentially acts as a low supply voltage output indicator.

Power-failure detection with auxiliary comparator

All devices have an auxiliary comparator with 1.25V trip point. The output, PFO, is active LOW and the noninverting input isPFI. This comparator can be used as a supply voltage monitor with an external resistor voltage divider. As the monitored voltage level falls, PFI is reduced causing the PFO output to go LOW. Normally PFO interrupts the processor so the system can be shut down in a controlled manner.



Watchdog Timing

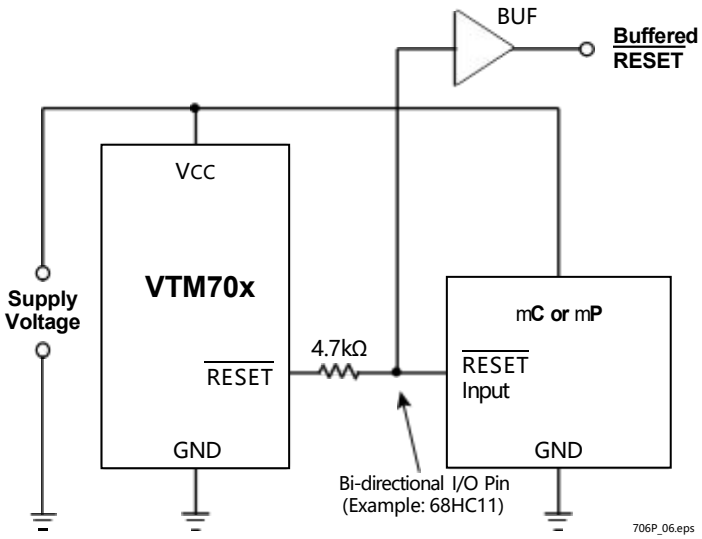


WDI Three-state operation

Application Information

Bi-directional Reset Pin Interfacing

The VTM706/8 can interface with µP/µC bi-directional reset pins by connecting a 4.7kΩ resistor in series with the RESET output and the µP/µCbi-directional reset pin.



Ensuring That $\overline{\text{RESET}}$ is Valid Down to V_{CC} = 0V

When V_{CC} falls below 1.2V, the VTM706R/S/T/J and VTM708R/S/T/J RESET reset outputs no longer pull down; it becomes indeterminate. To avoid the possibility that stray charges could build up and force RESET to the wrong state , a pull-down resistor should be connected to the RESET pin, thus draining such charges to ground. The resistor value is not critical. A 100kΩ resis-tor will pull RESET to ground without loading it.

Monitoring Voltages Other Than V_{CC}

The VTM706/708 can monitor voltages other than V_{CC} using the Power Fail circuitry. If a resistive divider ~~r is~~ connected from the voltage to be monitored to the PFI input, the PFO (output) will go LOW if the divider voltage goes below its 1.25V reference. Should hysteresis be desired, connect a resistor (equal to approxi~~mate~~ly 10 times the sum of the two resistors in the divider) between the PFI and PFO pins. A capacitor between PFI and GND will reduce circuit se~~nsiti~~vity to input high frequency noise. If it is de~~sired~~ to assert ~~a re~~set in addition to the PFO flag, this maybe achieved by connecting the PFO output to MR.

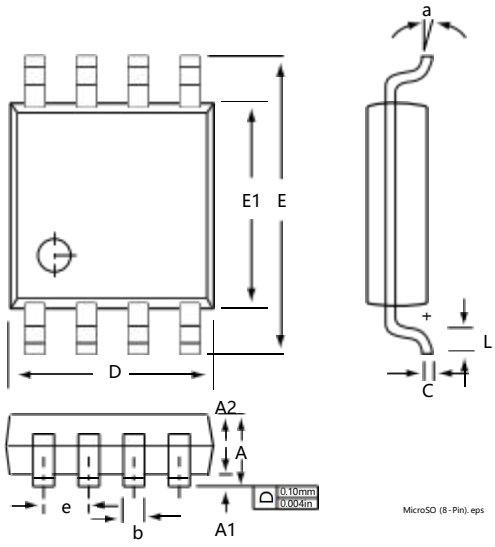
Package Dimensions

MicroSO (8-Pin)

	Inches		Millimeters	
	Min	Max	Min	Max
MicroSO (8-Pin)*				
A	———	0.0433	———	1.10
A1	0.0020	0.0059	0.050	0.15
A2	0.0295	0.0374	0.75	0.95
b	0.0098	0.0157	0.25	0.40
C	0.0051	0.0091	0.13	0.23
D	0.1142	0.1220	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.193 BSC		4.90 BSC	
E1	0.1142	0.1220	2.90	3.10
L	0.0157	0.0276	0.40	0.70
a	0°	6°	0°	6°

706P_t02a.at3

** JEDEC Drawing MO-187AA*



Package Dimensions

	Inches		Millimeters	
	Min	Max	Min	Max
SO (8-Pin)**				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	5.00
Plastic DIP (8-Pin)***				
A	———	0.210	——	5.33
A1	0.015	———	0.38	———
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	———	0.13	———
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	———	2.54	
eA	0.300	———	7.62	
eB	———	0.430	———	10.92
eC	———	0.060		
L	0.115	0.150	2.92	3.81

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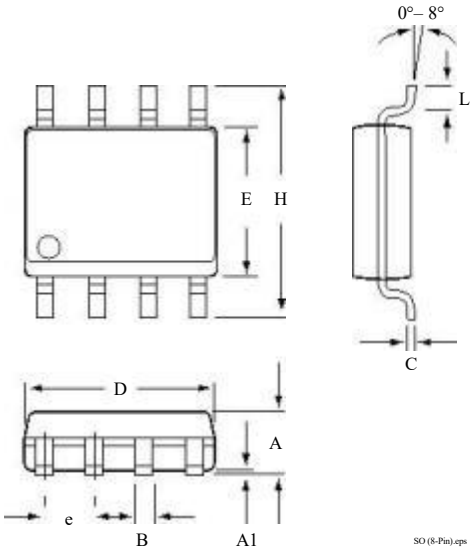
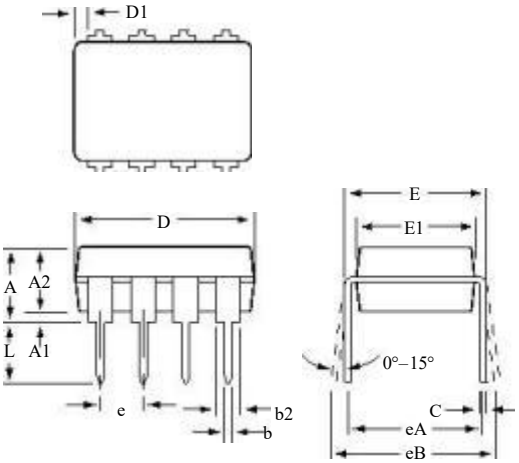
** JEDEC Drawing MS-112AA
*** JEDEC Drawing MS-001BA

SO (8-Pin)



SO (8-Pin).eps

Plastic DIP (8-Pin)



Plastic DIP (8-Pin)a.eps